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TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No. ITL.0286US

In Re Application Of: **David K. Vavro, et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/465,634	December 17, 1999	Tonia L. Meonske	47795	2181	9115

Invention: **Digital Signal Processor Having a Plurality of Independent Dedicated Processors**

COMMISSIONER FOR PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed on:

March 5, 2008

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Signature

Dated: **April 14, 2008**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	David K. Vavro, et al.	§	Art Unit:	2181
Serial No.:	09/465,634	§	Examiner:	Tonia L. Meonske
Filed:	December 17, 1999	§	Atty Docket:	ITL.0286US (P7814)
For:	Digital Signal Processor Having a Plurality of Independent Dedicated Processors	§	Assignee:	Intel Corporation

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APPEAL BRIEF

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Nancy Meshkoff

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REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

RELATED APPEALS AND INTERFERENCES

Appeal No. 2003-1635, decision mailed on September 17, 2004, for this application.

STATUS OF CLAIMS

Claims 1-4 (Rejected).

Claim 5 (Canceled).

Claims 6-7 (Rejected).

Claim 8 (Canceled).

Claims 9-16 (Rejected).

Claim 17 (Canceled).

Claims 18-24 (Rejected).

Claims 25-30 (Canceled).

Claims 1-4, 6-7, 9-16, and 18-24 are rejected and are the subject of this Appeal Brief.

STATUS OF AMENDMENTS

All amendments have been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

In the following discussion, the independent claims are read on one of many possible embodiments without limiting the claims:

1. A digital signal processor comprising:

a programmable, multiply and accumulate mathematical processor (Fig. 1, 30a; p. 5, lines 17-24);

an input processor that processes input signals to the digital signal processor (Fig. 1, 14; p. 4, lines 13-21);

an output processor that processes output signals from the digital signal processor (Fig. 1, 20; p. 4, lines 22-25);

a master processor that controls said mathematical processor, said input processor and said output processor provides the timing for the other processors (Fig. 1, 18; p. 4, lines 3-8);

a storage to store data from each of said processors so as to be selectively accessible by each of said processors (Fig. 1, 16; p. 6, lines 7-12); and

wherein each of said processors has a different instruction set than the other processors (p. 3, lines 16-17).

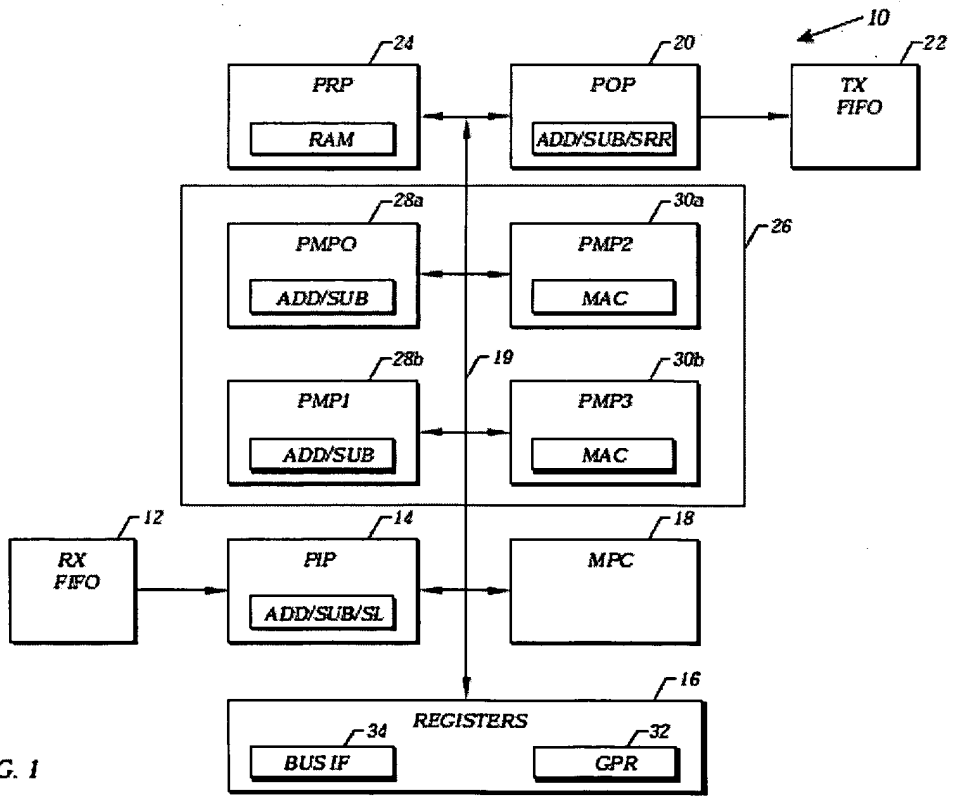

FIG. 1

7. The digital signal processor of claim 1 wherein each of said processors use very long instruction words (p. 5, lines 5-9).

16. A method of digital signal processing comprising:

using a first processor to process input signals to said digital signal processor (Fig. 1, 14; p. 4, lines 13-21);

using a second processor to process output signals from said signal digital signal processor (Fig. 1, 20; p. 4, lines 22-25);

using a third processor for multiply and accumulate operations (Fig. 1, 30a; p. 5, lines 17-24);

controlling said first, second and third processors using a fourth processor (Fig. 1, 18; p. 4, lines 3-8);

enabling each of said processors to store data in a storage and to selectively access said data stored in said storage by another one of said processors (Fig. 1, 16; p. 6, lines 7-12);

providing the timing from said fourth processor for each of the other processors (p. 4, lines 3-8); and

providing each of said processors with a different instruction set than the other processors (p. 3, lines 16-17).

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. **Whether claims 1-4, 6-7, 9-16, and 18-24 are anticipated under 35 U.S.C. § 103(a) by Balmer (US 5,197,140).**

ARGUMENT

A. Are claims 1-4, 6-7, 9-16, and 18-24 anticipated under 35 U.S.C. § 103(a) by Balmer (US 5,197,140)?

The cited reference fails to teach using different instruction sets, for each of three processors, as claimed and also fails to suggest using three different types of processors. Claim 1 is as follows:

> A digital signal processor comprising:
> a programmable, multiply and accumulate mathematical processor;
> an input processor that processes input signals to the digital signal processor;
> an output processor that processes output signals from the digital signal processor;
> a master processor that controls said mathematical processor, said input processor and said output processor provides the timing for the other processors;
> a storage to store data from each of said processors so as to be selectively accessible by each of said processors; and
> wherein each of said processors has a different instruction set than the other processors.

The last office action concedes that "Balmer has not specifically taught wherein each of said processors has a different instruction set then the other processors", apparently referring to the last clause of the above claim.

Despite the absence of any teaching in the cited art to meet the claimed invention, it is suggested that each processor has a different set of required tasks to make the system operate as described. Of course, every computer has a variety of different tasks to perform and that does not mean that it has to use a variety of different instruction sets.

Then it is argued that a customized processor with a unique instruction set that is only able to execute the required tasks is able to perform in an optimized and efficient manner. One problem with this statement is that it is based on nothing but hindsight reasoning.

This hindsight-reasoning-induced assertion is the sum total of all the reasoning provided in the rejection to assert obviousness based on a reference that clearly does not teach what is claimed. There is no reason that the processors could not be customized for their tasks without changing their instruction sets. That is, each processor could use exactly the same instruction set

and yet use that instruction set in a way to perform different tasks. Thus, not only is there no logical connection between the examiner's arguments and the finding of obviousness, there is technically no basis for the underlying premises.

For example, as set forth in the Computer Desktop Encyclopedia, an instruction set is "The repertoire of machine language instructions that a computer can follow (from a handful to several hundred). *See* Evidence Appendix. It is a major architectural component and is either built into the CPU or into microcode. Instructions are generally from one to four bytes long."

In effect, the rejection is based on nothing within the reference. There is no basis whatsoever to conclude that the instruction set of any processor within the reference is different from any other.

Therefore, the rejection should be reversed.

* * *

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: April 14, 2008

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CLAIMS APPENDIX

The claims on appeal are:

1. A digital signal processor comprising:

a programmable, multiply and accumulate mathematical processor;

an input processor that processes input signals to the digital signal processor;

an output processor that processes output signals from the digital signal processor;

a master processor that controls said mathematical processor, said input processor and said output processor provides the timing for the other processors;

a storage to store data from each of said processors so as to be selectively accessible by each of said processors; and

wherein each of said processors has a different instruction set than the other processors.

2. The digital signal processor of claim 1 further including a random access memory processor that stores intermediate calculation results.

3. The digital signal processor of claim 2 including a bus coupling each of said processors to said storage.

4. The digital signal processor of claim 1 wherein said input and output processors also implement mathematical operations.

6. The digital signal processor of claim 1 wherein said processors communicate with one another through said storage.

7. The digital signal processor of claim 1 wherein each of said processors use very long instruction words.

9. The digital signal processor of claim 1 wherein said master processor waits for the input processor to complete a given operation.

10. The digital signal processor of claim 1 wherein each of said processors includes its own random access memory.

11. The digital signal processor of claim 1 wherein said storage includes a plurality of registers, said registers automatically transfer existing data from a first register to a second register when new data is being written into said first register.

12. The digital signal processor of claim 11 wherein said input processor causes the automatic transfer of data.

13. The digital signal processor of claim 11 wherein said mathematical processor causes said data to be transferred from one register to another.

14. The digital signal processor of claim 1 including a mathematical processor which is pipelined.

15. The digital signal process of claim 1 wherein said mathematical processor is a multi-cycled mathematical processor.

16. A method of digital signal processing comprising:

using a first processor to process input signals to said digital signal processor;

using a second processor to process output signals from said signal digital signal processor;

using a third processor for multiply and accumulate operations;

controlling said first, second and third processors using a fourth processor;

enabling each of said processors to store data in a storage and to selectively access said data stored in said storage by another one of said processors;

providing the timing from said fourth processor for each of the other processors; and

providing each of said processors with a different instruction set than the other processors.

18. The method of claim 16 including automatically transferring data from a first register in said storage to a second register in said storage when new data is being written into said first register.

19. The method of claim 18 including automatically transferring said data in response to action by said first processor.

20. The method of claim 18 including automatically transferring said data in response to action by said third processor.

21. The method of claim 18 including storing a bit which indicates which processor may control said automatic transfer of data from one register to another.

22. The method of claim 16 including accommodating for timing differences between said processors by operating one of said processor in a pipelined fashion.

23. The method of claim 16 including accommodating differences in processing cycle time of one of said processors by operating said processor in a multi-cycle mode.

24. The method of claim 23 including holding off said fourth processor when one of said processors is taking more than a cycle to complete an instruction.

EVIDENCE APPENDIX

See entry for "instruction set", Computer Desktop Encyclopedia, on the following pages.

Computer Desktop Encyclopedia

Ninth Edition

Alan Freedman

Osborne/McGraw-Hill

New York Chicago San Francisco
Lisbon London Madrid Mexico City Milan
New Delhi San Juan Seoul Singapore Sydney Toronto

instance variable In object-oriented programming, a variable used by an instance of a class. It holds data for a particular object. Contrast with *class variable*. See *class*.

instantiate In object technology, to create an object of a specific class. See *instance*.

instant messaging A computer conference using the keyboard (a keyboard chat) over the Internet between two or more people. Instant messaging is not a dial-up system like the telephone; it requires that both parties be online at the same time. You have to put the names of people you want to instant message with in a list, and when any of those individuals log on, you are "instantly" notified so that you can begin an interactive chat session. AOL's Instant Messenger (AIM), Microsoft Network Messenger Service (MSNMS), ICQ and Yahoo! Messenger are the major instant messaging services.

In the business world, instant messaging is often used to avoid telephone tag, or to find out if a person is available to take a phone call. Many instant messaging sessions wind up as traditional telephone calls. However, instant messaging is expected to be the catalyst for IP-based phone calls initiated directly from the computer to provide a seamless move from typing to talking. See *IMUnified* and *Jabber*.

instant messenger The software that provides instant messaging services. See *instant messaging* and *AIM*.

instant print The ability to use the computer as a typewriter. Each keystroke is transferred to the printer.

instant replay See *PVR*.

Institute for Certification See *ICCP*.

instruction (1) A statement in a programming language.
(2) A machine instruction.

instruction cycle The time in which a single instruction is fetched from memory, decoded and executed. The first half of the cycle transfers the instruction from memory to the instruction register and decodes it. The second half executes the instruction.

instruction mix The blend of instruction types in a program. It often refers to writing generalized benchmarks, which requires that the amount of I/O versus processing versus math instructions, etc., reflects the type of application the benchmark is written for.

instruction register A high-speed circuit that holds an instruction for decoding and execution.

instruction repertoire Same as *instruction set*.

instruction set The repertoire of machine language instructions that a computer can follow (from a handful to several hundred). It is a major architectural component and is either built into the CPU or into microcode. Instructions are generally from one to four bytes long.

instruction time The time in which an instruction is fetched from memory and stored in the instruction register. It is the first half of the instruction cycle.

insulator A material that does not conduct electricity. Contrast with *conductor*.

int A programming statement that specifies an interrupt or that declares an integer variable. See *interrupt* and *integer*.

int 13 A DOS interrupt used to activate disk functions, such as seek, read, write and format.

int 14 A DOS interrupt used to activate functions on the serial port (COM1, COM2, etc.). See *NASI*.

RELATED PROCEEDINGS APPENDIX

See Decision on Appeal No. 2003-1635, mailed September 17, 2004, for this application, on the following pages.

ITL.02864US
P7814

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DAVID K. VAVRO and JAMES A. MITCHELL

Appeal No. 2003-1635
Application No. 09/465,634

ON BRIEF

Before FLEMING, DIXON, and GROSS, ***Administrative Patent Judges***.
GROSS, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1 through 24, which are all of the claims pending in this application.

Appellants' invention relates to a digital signal processor with several individual processors including a master processor which controls the other processors. Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A digital signal processor comprising:

a mathematical processor;

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Due Date 11-17-04
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an input processor that processes input signals to the digital signal processor;

an output processor that processes output signals from the digital signal processor;

a master processor that controls said mathematical processor, said input processor and said output processor; and

a storage selectively accessible by each of said processors.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Nakagawa et al. (Nakagawa)	5,241,679	Aug. 31, 1993
Whittaker et al. (Whittaker)	5,968,167	Oct. 19, 1999
Kitamura	EP0942603	Sep. 15, 1999

Claim 15 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Claims 1 through 4, 6, 8, 9, 15 through 17, 23, and 24 stand rejected under 35 U.S.C. § 102(a) as being anticipated by Kitamura.

Claims 5, 7, 14, and 22 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kitamura.

Claim 10 stands rejected under 35 U.S.C. § 103 as being unpatentable over Kitamura in view of Whittaker.

Claims 11 through 13 and 18 through 21 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kitamura in view of Nakagawa.

Reference is made to the Examiner's Answer (Paper No. 11, mailed February 11, 2002) for the examiner's complete reasoning in support of the rejections, and to appellants' Brief (Paper No. 10, filed January 22, 2003) for appellants' arguments thereagainst.

OPINION

As a preliminary matter, we note that appellants indicate on page 15 of the Brief that claims 1 through 15 are to be grouped together, but separately from claims 16 through 24, which are also to be grouped together. However, the argument presented for claim 16 (Brief, page 17) is identical to the argument presented for claim 1 (Brief, pages 16-17). Therefore, appellants have failed to present separate arguments in accordance with 37 C.F.R. § 1.192(c)(7) (which was in effect at the time of the Brief). Accordingly, we shall group claim 16 and its dependents with claim 1 and its dependents.

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellants and the examiner. As a consequence of our review, we will reverse the indefiniteness rejection of claim 15. In addition, we will affirm the anticipation rejection of claims 1

through 4, 6, 8, 9, 15 through 17, 23, and 24 and the obviousness rejections of claims 5, 7, 10 through 14, and 18 through 22.

Regarding the rejection of claim 15 under 35 U.S.C. § 112, second paragraph, the examiner asserts (Answer, page 11) that there are two ways to interpret "multi-cycled mathematical processor." The examiner directs our attention to appellants' specification, page 24, lines 20-23, as support for one interpretation, that "the processor requires multiple cycles to complete an operation," and to page 23, line 19, for the other interpretation, that "it is operated at various cycle speeds." Although we agree with the examiner's interpretation of the page 24 excerpt, we disagree with the interpretation of the page 23 excerpt. The portion referenced on page 23 also suggests that the processor requires multiple cycles, though they may also be at different speeds due to the "self-timed" aspect. Accordingly, we find claim 15 to be definite, and we will reverse the rejection under 35 U.S.C. § 112, second paragraph.

As to the anticipation rejection of claims 1 through 4, 6, 8, 9, 15 through 17, 23, and 24, appellants' sole argument (Brief, pages 16-17) is that Kitamura fails to disclose a mathematical processor. Appellants assert (Brief, page 16) that data processing unit 5 (the element the examiner gave as a

mathematical processor (Answer, page 4)) splices video data, and "[t]here is no indication that this device can be considered to be a mathematical processor."

The examiner explains (Answer, pages 12-13) that data processing unit 5 acts upon encoded video data DA and DB, "which are combinations of bits, or numbers." The examiner contends that acting upon bits or numbers constitutes mathematical operations. Further, the examiner asserts that the blanking generator 20, which is part of processing unit 5, sets a differential value between two macroblocks, and thereby performs subtraction, a mathematical operation. Accordingly, the examiner concludes that data processing unit 5 is a mathematical processor.

Appellants do not provide a definition of a mathematical processor in the specification. Instead, appellants (page 5, lines 17-23) provide examples of mathematical processors including add and subtract and multiply and accumulate processors. Appellants add that other mathematical processors may be used based on the particular needs in particular applications. Thus, appellants suggest that there are other types of mathematical processors and that the invention is not limited to the examples given in the specification.

We find that the examiner clearly explained how Kitamura's processor 5 does mathematical functions. In addition, Figure 20 further shows how the operations of the blanking generator are mathematical functions. Therefore, we agree with the examiner that since processor 5 acts on bits or numbers, and since the blanking generator is part of processor 5 and performs mathematical operations, processor 5 is a mathematical processor. Consequently, we will sustain the anticipation rejection of claims 1 through 4, 6, 8, 9, 15 through 17, 23, and 24.

Appellants presented no further arguments for the obviousness rejection of claims 5, 7, 14, and 22 over Kitamura alone, nor for the addition of Whittaker for the rejection of claim 10, nor for the addition of Nakagawa for the rejection of claims 11 through 13 and 18 through 21. Therefore, we will affirm the rejections of claims 5, 7, 10 through 14 and 18 through 22 for substantially the same reasons as explained ***supra***.

CONCLUSION

The decision of the examiner rejecting claim 15 under 35 U.S.C. § 112, second paragraph is reversed. The decision of the examiner rejecting claims 1 through 4, 6, 8, 9, 15 through

17, 23, and 24 under 35 U.S.C. § 102(a) and claims 5, 7, 10 through 14, and 18 through 22 under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

MICHAEL R. FLEMING
Administrative Patent Judge

JOSEPH L. DIXON
Administrative Patent Judge

ANITA PELLMAN GROSS
Administrative Patent Judge

BOARD OF PATENT APPEALS AND INTERFERENCES

APG:clm

Appeal No. 2003-1635
Application No. 09/465,634

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